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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/750,198 | 12/27/2000 | Anil Vasudevan | 042390.P9018 | 7014 |

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| EXAMINER |
|---|
| HUYNH, KIM T |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2189 | 2 |

DATE MAILED: 07/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/750,198 | VASUDEVAN, ANIL | |
| | Examiner | Art Unit | |
| | Kim T. Huynh | 2189 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12/27/00* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-14 and 16-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14, 16-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Objections*

1. Content of Specification

Sequence Listing, See 37 CFR 1.821-1.825 and MPEP §§ 2421-2431. The requirement for a sequence listing applies to all sequences disclosed in a given application, whether the sequences are claimed or not. See MPEP § 2421.02.

Claim 15 is missing. Renumbered the claims. Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-14, 16-20 rejected under 35 U.S.C. 102(e) as being anticipated by Chiloyan et al. (Pub. No.: US 20020083228)

a. As per claim 1, Chiloyan discloses an apparatus comprising:

- a housing; (fig.1), [0061]
- a mainboard(fig.1, 20) including memory (fig.1, 24) and a first processor (fig.1, 21) mounted within the housing; [0061]
- a first network interface having a first network port and a first address connected to the first processor;[0030]

- at least one expansion slot (fig.1, 46) for receiving a peripheral device; (fgi.1, 56) and
- a network communications link connecting the first network interface to said at least one expansion slot substantially disposed within the housing,[0032]
- wherein the first processor is enabled to communicate with a peripheral device having a build-in network interface by transmitting data via the first network interface and the built-in network interface over the network communications link using a network communications link using a network transmission protocol.[0030],[0032],[0034],[0039]

b. As per claim 2, Chiloyan discloses apparatus further comprising a second network interface disposed on the mainboard in proximity to said at least one expansion slot having a second address and a second network port to enable communication between the first processor and a peripheral device that does not include a built-in network interface when the peripheral device is mounted in one of said at least one expansion slots.[0030],[0031]

c. As per claim 3, Chiloyan discloses wherein the network communications link comprises a network bus (fig.1, 23) embedded in the mainboard(fig.1,20).

d. As per claims 4, 7, 9 and 20, Chiloyan discloses wherein the first network interface and the communications link comprise an Ethernet subnet, Token-ring (fig.1,53), [0032]

e. As per claim 5, Chiloyan discloses an apparatus further comprising:

- a second processor; and ([0016],[0035], wherein processing inherently from device driver)
- a second network interface connected to the second processor and the network communications link to enable communication between the second processor and a peripheral device having a built-in network interface.[0016],[0017],[0030]

f. As per claim 6, Chiloyan discloses a system comprising:

- a computing machine including a housing and a mainboard to which memory and a first processor are connected, providing a first network interface having a first network port and a first address;[0032]
- a first peripheral device disposed within the housing;[0002],[0034]
- a second network interface providing a second network port and a second network address linked in communication with the first peripheral device;[0032]
- a communication link between the first and second network interfaces substantially disposed within the housing; and [0002],[0034]
- software comprising machine instructions that are executable by the first processor that includes a socket application interface (API) that binds the address of the first peripheral device to the second network port and a network interface abstraction layer that provides an abstracted interface that enables an application to communicate with the first peripheral device using a network protocol.[0016],[0028]

g. As per claim 8, Chiloyan discloses wherein the communication link comprises a network signal bus built into the mainboard. [0034]

h. As per claim 10, wherein the second network interface is built into the first peripheral device;[0030]

i. As per claim 11, Chiloyan discloses wherein the second network interface is built into the mainboard.(fig.1, 53)

j. As per claim 12, Chiloyan discloses wherein the peripheral device comprises one of a video subsystem, a memory, a disk controller and a modem.(fig.1, 32)

k. As per claim 13, Chiloyan discloses wherein the mainboard further includes a second processor connected to a third network interface having a third network address and network port connected to the communications link.[0008], [0016],[0030]

l. As per claim 14, Chiloyan discloses a method for enabling communication between a peripheral device disposed within a computing machine having a processor and an application running on the processor, comprising :

- providing a network interface for each of the processor and the peripheral device; [0035]
- providing a communication link between the network interfaces of the processor and the peripheral device;[0032]
- creating a network socket for each of the processor and the peripheral device; [0030]

- stabling a connection between the processor and the peripheral device;[0034]
- generating messages with the application;[0047],[0030]
- transferring the messages between the processor and peripheral device using a network transmission protocol.[0047],[0030],[0011]

m. As per claim 16, Chiloyan discloses wherein the network transmission protocol comprises the TCP/IP protocol. [0039],[0034]

n. As per claim 17, Chiloyan discloses the method further comprising applying security measures to determine if an application may connect to a particular peripheral device.[0001], wherein identifier implies security)

o. As per claim 18, Chiloyan discloses wherein the network transmission protocol comprises the UDP protocol. [0039]

p. As per claim 19, Chiloyan discloses wherein the communications link and the network interfaces comprise an internal Ethernet network. [0032]

***Conclusion***

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Abler et al. [Pub. No. US 20030067884] discloses LAN network protocol

Anand et al. [USPN 6,370,599] discloses network interface card peripheral

*4. A shortened statutory period for reply is set to expire THREE months from the mailing date of this communication. Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) months from the mailing date of this communication. If the period for reply specified above is less than thirty (30) days, a reply within the*

*statutory minimum of thirty (30) days will be considered timely. If no period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) months from the mailing date of this communication. Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C 133).*

*Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).*

*5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 8:30AM- 6:30PM.*

*If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815 or via e-mail addressed to [mark.rinehart@uspto.gov]. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-7249 for regular communications and (703)746-7238 for After Final communications.*

*Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.*

*Kim Huynh*

*June 26, 2003*

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100